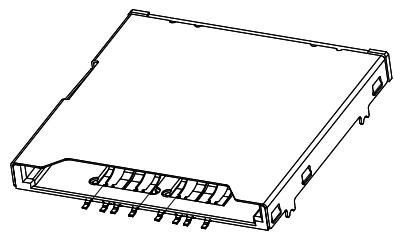


PAD AREA
 NO COPPER AREA (NO TRACE & VIA & GND)
 MANY GND VIA
 SURFACE COPPER POUR AREA

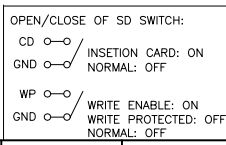
RECOMMENDED PCB LAYOUT(TOP VIEW)
TOLERANCE:±0.05mm

- NOTES :
- MATERIAL :
 - HOUSING:LCP UL94 V-0, BLACK COLOR.
 - SHELL: STAINLESS STEEL
 - CONTACT: COPPER ALLOY
 - FINISH :
 - CONTACT: GOLD PLATING ON CONTACT AREA, GOLD FLASH ON SOLDERTAIL AREA. 50u" MIN NICKEL PLATING OVERALL.
 - SHELL: 30u" MIN SOLDERABLE NICKEL PLATING OVERALL.
 - ELECTRICAL CHARACTERISTICS:
 - OPERATING VOLTAGE : 100V AC(rms)/DC.
 - CURRENT RATING : 0.5 A.
 - OPERATING TEMPERATURE: -25°C~+85°C.
 - CONTACT RESISTANCE: 100 m OHMS MAX.
 - INSULATION RESISTANCE: 1000M OHMS MIN. AT 250VDC.
 - DIELECTRIC WITHSTANDING VOLTAGE:500 VAC/1MINUTE.



Pin Define

PIN NO.	SD Mode			UHS-II Mode			PCIe Mode		
	Name	Type	Discription	Name	Type	Discription	Name	Type	Discription
Pin 1	CD/DAT3	I/O/PP	Card Detect/Data Line[Bit3]	-	-	Not used	PERST#	I	PE Reset is a functional reset
Pin 2	CMD	PP	Command/Response	-	-	Not used	-	-	Not used
Pin 3	VSS1	S	Supply Voltage Ground	VSS1	S	Supply Voltage Ground	VSS1	S	Supply Voltage Ground
Pin 4	VDD	S	Supply Voltage	VDD1	S	Supply Voltage (3.3V)	VDD1	S	Supply Voltage (3.3V)
Pin 5	CLK	I	Clock	-	-	Not used	-	-	Not used
Pin 6	VSS2	S	Supply Voltage Ground	VSS2	S	Supply Voltage Ground	VSS2	S	Supply Voltage Ground
Pin 7	DAT0	I/O/PP	Data Line[Bit0]	RCLK+	I		REFCLK+	IDS	PCIe Ref Clock
Pin 8	DAT1	I/O/PP	Data Line[Bit1]	RCLK-	I		REFCLK-	IDS	PCIe Ref Clock
Pin 9	DAT2	I/O/PP	Data Line[Bit2]	-	-		CLKREQ#	I/O/D/D	Reference clock request signal, Also used by L1 PM substates
Pin 10	-	-	Not used(Connected to Ground)	VSS3	S	Supply Voltage Ground	VSS3	S	Supply Voltage Ground
Pin 11	-	-	Not used	D0+	LVDS		PCIe TX0+	IDS	Card input (land 0)
Pin 12	-	-	Not used	D0-	LVDS		PCIe TX0-	IDS	Card input (land 0)
Pin 13	-	-	Not used(Connected to Ground)	VSS4	S	Supply Voltage Ground	VSS4	S	Supply Voltage Ground
Pin 14	-	-	Not used	VDD2	S	Supply Voltage (1.8V)	VDD2	S	Supply Voltage (1.8V)
Pin 15	-	-	Not used	D1-	LVDS		PCIe RX0-	DDS	Card output (land 0)
Pin 16	-	-	Not used	D1+	LVDS		PCIe RX0+	DDS	Card output (land 0)
Pin 17	-	-	Not used(Connected to Ground)	VSS5	S	Supply Voltage Ground	VSS5	S	Supply Voltage Ground
Pin 18	-	-	Not used	-	-	-	VDD3	S	Supply Voltage (1.2V)
Pin 19	-	-	Not used	-	-	-	VDD1a	S	Supply Voltage (3.3V)
Pin 20	-	-	Not used	-	-	-	VSS6	S	Supply Voltage Ground
Pin 21	-	-	Not used	-	-	-	PCIe TX1+	IDS	Card input (land 1)
Pin 22	-	-	Not used	-	-	-	PCIe TX1-	IDS	Card input (land 1)
Pin 23	-	-	Not used	-	-	-	VSS7	S	Supply Voltage Ground
Pin 24	-	-	Not used	-	-	-	VDD2a	S	Supply Voltage (1.8V)
Pin 25	-	-	Not used	-	-	-	PCIe RX1-	DDS	Card output (land 1)
Pin 26	-	-	Not used	-	-	-	PCIe RX1+	DDS	Card output (land 1)
Pin 27	-	-	Not used	-	-	-	VSS8	S	Supply Voltage Ground



- PART.NO.: TW266-AN401-**-**
- 08: 功能区镀金10", 锡脚Gold Flash
 - 09: 功能区镀金50", 锡脚Gold Flash
 - 10: 功能区镀金150", 锡脚Gold Flash
 - 11: 功能区镀金150", 锡脚Gold Flash
 - 12: 功能区镀金300", 锡脚Gold Flash

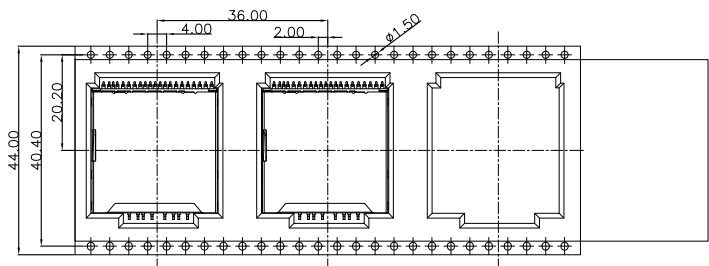
GENERAL TOLERANCE	TW266-AN401-00	DWG.NO.	TW266-AN401-00	PART.NO.	TW266-AN401-**-**	DRAWN	Jason 2023.07.18	UNIT	mm	SCALE	1:1
x:±0.50	x:±5°	REV.	A	TITLE	SD8.0 No Push H2.95 conn.	CHECKED		东莞市欧联电子科技有限公司 DONGGUAN OLN ELECTRONICS TECHNOLOGY CO., LTD.			
.x±0.38	.x±2°	SIZE	A4	SHEET	1/2	APPROVED					
.xx±0.25	.xx±1°	A4									

东莞市欧联电子科技有限公司

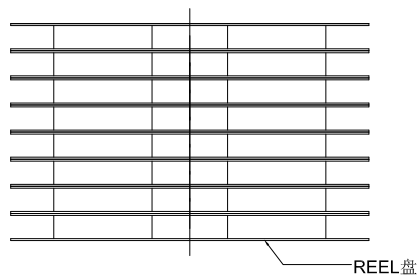
包装作业规范

包装作业图示及说明 (PACKING OPERATION DIAGRAM & INSTRUCTION)

- 一.
- 1) 将成品一一放入REEL包装盘内,依同一方向放入.
 - 2) 包装时,如图所示.
 - 3) 一个REEL包装盘放置500个成品.



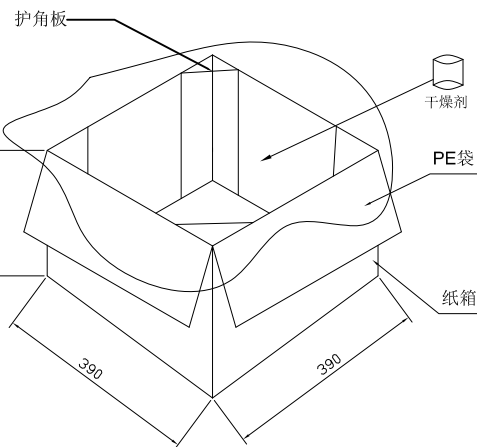
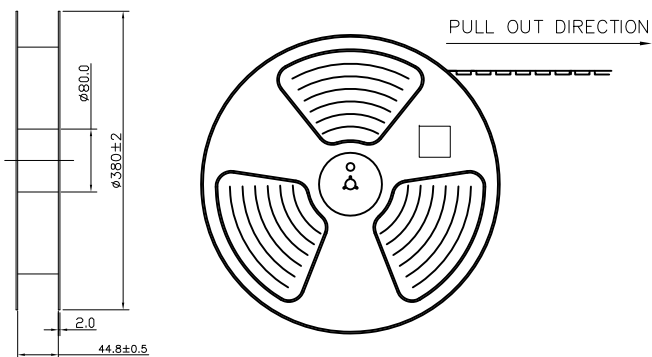
- 三.
- 1) 每箱装 6 盘REEL包装盘.
 - 2) 每箱放置 2400 PCS 的成品.



- 四.
- 1) 用TAPE将纸箱封实.



- 二.
- 1) 装盘前先把前面空20pcs产品,然后再开始装盘,尾端也需空20pcs产品,上带加长200mm.
 - 2) 装满成品的REEL包装盘如下图所示.



備註 (REMARK)

1. 若有未装满之零数箱,必须以缓冲材塞满.

GENERAL TOLERANCE	DWG.ND.	TW266-AN401-00	PART.ND.	TW266-AN401-**	DRAWN	Jason 2023.07.18
x:±0.50	REV.	A	TITLE	SD8.0 No Push H2.95 conn.	CHECKED	
.x±0.38	SIZE		SHEET	2/2	APPROVED	
.xx±0.25	A4					

UNIT	mm	SCALE	1:1
东莞市欧联电子科技有限公司 DONGGUAN OLN ELECTRONICS TECHNOLOGY CO., LTD.			